AMENDMENTS IN THE SPECIFICATION

Please replace paragraph **[0025]** *with the following:*

As depicted in **Figure 4**, the self-test system **48** includes a random digital sequence generator **52** which issues a series of digital "1" and "0" bits in a random sequence. A suitable random digital sequence generator **52**, for example, takes the form of a linear feedback shift register to generate the random sequence of digital bits. The random output sequence of digital bits from the generator **52** is furnished to an activate circuit **54**. In one embodiment, the random digital sequence generator **52** and the activate circuit **54** are included within a single component, referred to as the activator **51**. As will be set forth, the activate circuit **54** includes a time adjust system **56** (**Figure 5**) which, on receipt of signals on line **50** introduces time delay or jitter in the data windows. At such times, the activate circuit **54** sends test data in the form of the random digital sequence from generator **52**, but in data windows or eyes which are delayed in the opening or advanced in their closing, or both, like the data windows **14** of **Figure 2**.

Please replace paragraph **[0035]** *with the following:*

Figure 5 in the drawings depicts a preferred embodiment of the activate circuit **54**. The incoming stream of bits, whether SYSTEM DATA or a random series of bits from the random sequence generator **52**, is fed to each of a pair of latches **63** and **65**. The latches **63** and **65** are set to operate and store alternating bits, "ODD" and "EVEN", in the sequence of bits received from the generator **52**. Latch **63** is termed an even bit latch and latch **65** is termed an odd bit latch. The latches **63** and **65** are connected to a multiplexer **66** where the alternating bits are recombined. Thus, either ~~SYSTEMDATA~~ SYSTEM DATA or serial test data in the recombined form of the original random bit sequence from the generator **52**, is presented to the multiplexer **60**. The multiplexer **60** allows the bit sequence to pass to an amplifier of driver **62** and to an amplifier in driver **64**.

Please replace paragraph **[0037]** *with the following:*

A decode gating circuit **80** is connected to the outputs of each of the four latches [[**62**]] **63**, [[**64**]] **65**, **74** and **76**. The decode gating circuit **80** is configured to indicate when the

selected sequence of bits described above is present. As has been set forth, in the preferred embodiment, the desired sequence is the presence of either four consecutive "1" bits or 1111, or four consecutive "0" bits, or 0000, in the output from the generator **52**. Thus, in the preferred embodiment a logic element or function **82** detects the presence of the 1111 bits in the four latches and forms a FOUR ONES signal at its output. The FOUR ONES output of logic element **82** is furnished to a stretcher or delay circuit **83** formed by a latch **83A**, a delay element **83B** having a delay of 1/4 of a bit period, and an OR element or function **83C**. The latch **83A** delays the output of logic **82** by 2 bit periods.

Please replace paragraph **[0041]** *with the following:*

The outputs from the logic function **98**, **100** and **102** are furnished to an OR logic function **104** which in turn is connected to the multiplexor **60**. The multiplexor **60** is arranged to normally pass serial data, as has been set forth. In the event of an activation indication from line **50** to add jitter, the multiplexor **60** instead allows signals to pass to an amplifier in drivers [[**70**]] **62** and [[**72**]] **64** according to the logic functions performed in the gating circuit **80**. The operation of the logic functions in gating circuit **80** may be implemented by individual logic elements as shown schematically in the drawings or in an application specific integrating circuit or ASIC or some other arrangement according to the following logic equation: